Design and Simulation Fractional-N Phase Locked Loop Frequency Synthesizer using Sigma-Delta modulator for Bluetooth Systems

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Abstract*—Phase locked loop is a technique usually used to perform indirect digital frequency synthesizer for most RF transceivers. A fractional-N phase locked loop frequency synthesizer has been used in recent years since it achieves fine resolution and large loop bandwidth . This paper presents the design and simulation of a fractional-N phase locked loop frequency synthesizer using sigma-delta modulation for bluetooth standard systems with a frequency range from 2402 to 2480MHz. Loop filter and Sigma-Delta modulator are the most important factors in improving the performance of fractional-N phase locked loop. The digital Sigma-Delta modulator provides a useful noise shaping for the phase noise introduced by the fractional division operation, while the loop filter bandwidth limits the speed of switching time between the synthesized frequencies. A forth order passive loop filter was implemented at bandwidth equal to 200 KHz, 50° phase margin, and a second order single loop modulator with 4-level quantizer was used to control the frequency divider. Simulation results showed that the system is stable, and there is no fractional spurs in the output spectrum of the fractional-N phase locked loop.*

Keywords*-Phase Locked Loop; Sigma-Delta modulation; Frequency Synthesizer; Fractional-N; Phase Noise*

I. INTRODUCTION

A phase locked loop (PLL) can be divided into two architectures, an integer-N PLL and a fractional-N PLL. The main problem of the integer-N PLL is the trade-off between the channel spacing(frequency resolution) and the loop bandwidth. A small channel spacing or high frequency resolution requires a small reference frequency (F_{ref}), but using a small reference frequency leads to two main issues. First, for stability requirement the loop bandwidth must be smaller than the reference frequency ($f_{B.W} \ll 0.1\, F_{ref}$), therefore a low reference frequency means a small loop bandwidth, and this will result in slow switching time. Second, reducing the reference frequency causes an increase in the phase noise because of the high division ratio[1]. The fractional-N PLL solves the trade-off issue found in the integer-N PLL, offering a lower phase noise, higher frequency resolution, and a larger loop bandwidth. A larger loop bandwidth means faster switching time[2]. The output frequency of the fractional-N PLL is $f_{out}=(N.\alpha)*F_{ref}$, where N is an integer, and α is the fractional part. A dual modulus divider is used to average many integer divider cycles over time to obtain the desired fractional division ratio. A simple digitalaccumulator with an overflow controlling the dual modulus divider can be used to get the fractional ratio[3].Themain problem of this method is that the periodic operation of the dual modulus divider generates a spurious tones that is called fractional spurs[4].The first fractional spurs located at ($\alpha.F_{ref}$); if these spurs appear inside the loop bandwidth, this problem can be solved by reducing the loop bandwidth to remove these spurs, but this will increase the switching time. The best method to remove the fractional spurs without affecting the loop bandwidth is by breaking the periodicity of the dual modulus operation, which is realized by using a Sigma-Delta Modulation technique.

The Sigma-Delta modulator changes the division ratio between more than two values, so the spurs will spread over the spectrum. The Sigma-Delta modulator generates a random integer number with an average equal to the desired fractional ratio(while shaping the quantization noise) and pushes the spurious contents to the higher frequencies. Then the spurious contents are removed by the loop filter action [3,5].

II. SIGMA-DELTA FRACTIONAL-N FREQUENCY SYNTHESIZER BACKGROUND

A block diagram of the fractional-N PLL frequency synthesizer and the Sigma-Delta Modulation technique is shown in Fig 1,which consists of Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO),and Sigma-Delta modulator. The aim of using fractional-N PLL is to produce a periodic waveform that is fractional multiples of the reference oscillator (F_{ref}).

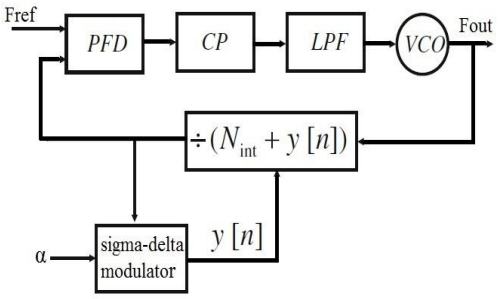

Figure 1. Block diagram of Sigma-Delta Fractional-N PLL [6]

The input of Sigma-Delta modulator is the desired fractional division number (α), where the output consists of a DC component y[n] that is proportional to the input (α),plus the quantization noise introduced due to using integer divider instead of ideal fractional divider. The frequency divider divides the output frequency (Fout) of the VCO by N_{int}+y[n], where N_{int} is an integer value, and y[n] is the output sequence of the modulator.The operation of the Sigma-Delta modulator is based on the noise shaping and oversampling property, which means that the quantization noise around the desired band signal is suppressed by using an integrator and a negative feedback[6].Fig 2 shows the first order Sigma-Delta modulator, which consists of one difference operator, one unit delay, one discrete integrator, and one bit quantizer[7].The relation between the input and output is given by:

$$Y(z) = X(z) + (1-z^{-1})\,Q(z). \qquad (1)$$

The feedback loop shapes the quantization noise in proportion to $(1-z^{-1})$; in other word the error introduced from the quantizer is pushed to the high frequencies due to the term $(1-z^{-1})$, where the input signal to the modulator is oversampled [8]. The noise shaping property is discussed in reference [9] and the key equations are shown here:

$$\frac{Y(z)}{Q(z)} = 1-z^{-1} \qquad (2)$$

Where $z = e^{j2\pi fT_{ck}}$, then

$$\frac{Y(z)}{Q(z)} = (1 - e^{-j2\pi fT_{ck}}) \qquad (3)$$

$$\frac{Y(z)}{Q(z)} = e^{-j\pi fT_{ck}}\,(e^{j\pi fT_{ck}} - e^{-j\pi fT_{ck}}) \qquad (4)$$

$$\frac{Y(z)}{Q(z)} = 2.j.e^{-j\pi fT_{ck}}\sin(\pi fT_{ck}) \qquad (5)$$

Hence the noise shaping function is written as:

$$S_y(f) = S_q(f)\,|2\,\sin(\pi fT_{ck})|^2 \qquad (6)$$

$$S_y(f) = 2\,S_q(f)\,|1 - \cos(2\,\pi\,f\,T_{ck})\,| \qquad (7)$$

Where:

T_{ck}:- clock frequency of Sigma-Delta modulator.

$$fs = \frac{1}{T_{ck}} \text{(sampling frequency of Sigma-Delta modulator)}$$

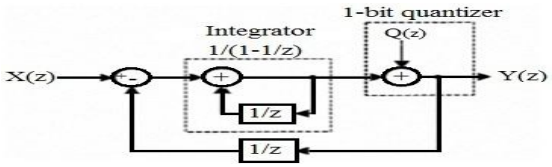

Figure 2. First Order Sigma-Delta Modulator [7]

Fig3 shows the spectrum of a first order Sigma-Delta noise shaping.

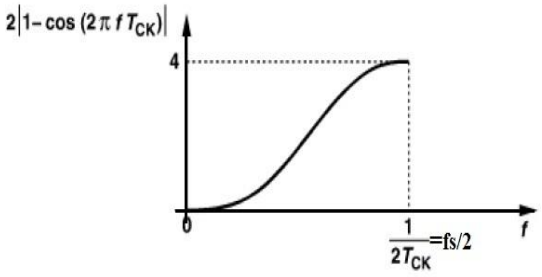

Figure 3. Noise shaping of the 1st Order Modulator[9]

Where $S_q(f)$ is relatively flat for the frequency range of interest.The second order Sigma-Delta modulator is shown in Fig 4, where the noise transfer function is:

$$\frac{Y(z)}{Q(z)} = (1 - z^{-1})^2 \qquad (8)$$

The noise shaping function is:

$$S_y(f) = S_q(f)|2\sin(\pi f T_{ck})|^4 \qquad (9)$$

The second order Sigma-Delta modulator provides better noise shaping than the first order as shown in Fig 5.

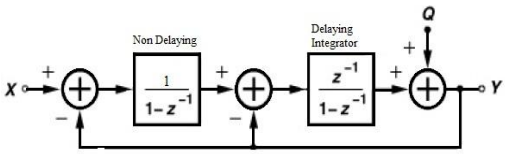

Figure 4. Second Order Sigma-Delta Modulator [9]

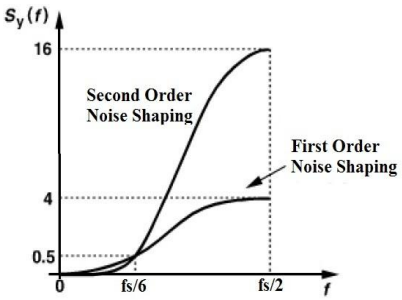

Figure 5. Noise Shaping of 1st and 2nd Order Modulator[9]

It is clear from the above figure that at frequenciesf $>\frac{fs}{6}$, the quantization noise increases as frequency increases, depending on the order of modulator[2].It isworth pointing out that the quantization noise limits the bandwidth of the fractional-N PLL, therefore the loop bandwidth must be chosen carefully to provide the best suppression of the quantization noise[10].

III. DESIGN AND SIMULATION METHODS

The proposed Sigma-Delta fractional-N frequency synthesizer used in this paper is shown in Fig 6.

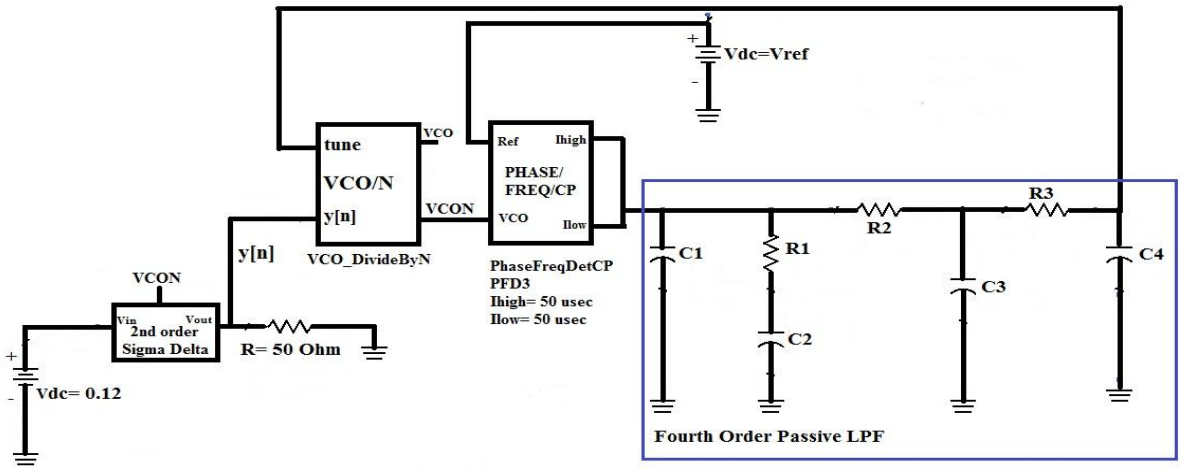

Figure 6. A circuit of the Sigma-Delta Fractional-N Frequency Synthesizer

This study focuses on the design of the loop filter and the Sigma-Delta modulator to improve the performance of the frequency synthesizer. The proposed architecture is designed to work at bluetooth frequencies in the range of 2402 to 2480 MHz with a channel spacing = 1 MHz. The channel spacing specifies the distance between the channels, so the output frequency will be increased by 1 MHz . The reference frequency used is 25 MHz.

A second order single loop Sigma-Delta modulator with 4-level quantizer was used to modulate the desired fractional ratio (α). The modulator, shown in Fig 7, consists of two difference operators, two integrators, multibit quantizer, and a negative feedback. This modulator generates a sequence of random integer number in the form -1,0,1,2,0,1,-1,2, ….., so the division ratio changes as 95, 96, 97, 98, 96, 97, 95, 98, …..as shown in Fig8. The relationship between the input and output isdescribed by the following equations:

$$V_o(z) = V_{in}(z).\, z^{-2} + E_n\,(1 - z^{-1})^2 \quad (10)$$

Where E_n is the quantization noise of the quantizer

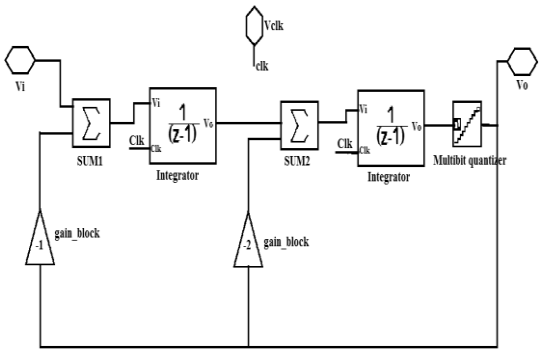

Figure 7. Second Order Sigma-Delta Modulator

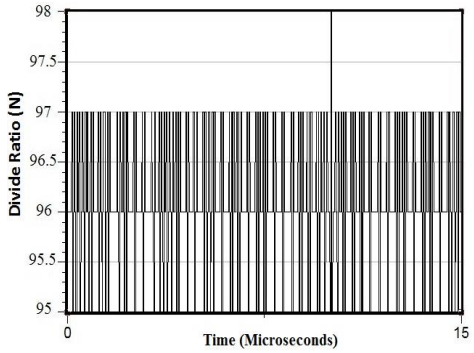

Figure 8. Divide Ratio (N)

A fourth order passive loop filter was implemented to have a 200 KHz bandwidth, and 50° phase margin. This filter provides an effective filtering for the reference spurs, and the noise with offset equal to at least twenty times the loop bandwidth. The design process is very complicated due to the difficulty in designing a stable loop filter that has all real components[11]. The loop filter was designed using Dean Banerjee equations andthe average current to voltage transfer function of the loop filter isdescribed as follows[11]:

$$H(s)=\frac{1+s.T2}{s(A3.s^3+A2.s^2+A1.s+A0)} \quad (11)$$

Where:

T2 is the zero of the filter = R1.C2(12)

$$A3=C1.C2.C3.C4.R1.R2.R3 \quad (13)$$

A2=C1.C2.R1.R2(C3+C4)

+C4.R3(C2.C3.R2+C1.C3.R2+

C1.C2.R1+C2.C3.R1) (14)

A1= C2.R1.(C1+C2+C3)+R2.(C1+C2)

.(C3+C4)+C4.R3(C1+C2+C3)(15)

$$A0= C1+C2+C3+C4 \quad (16)$$

$$A0=\frac{K_\phi.K_{vco}}{wc^2.N}\sqrt{\frac{1+wc^2.T2^2}{(1+wc^2.T1^2).(1+wc^2.T3^2).(1+wc^2.T4^2)}} \quad (17)$$

$K_{vco}$is the gain of the voltage controlled oscillator, K_ϕ is the charge pump current, (T1, T3, T4) are thepoles of the loop filter. The equations of loop filter components are:

$$C1=\frac{a2}{T2^2}\left(1+\sqrt{\left(1+\frac{T2}{a2}\right).(T2.A0-a1)}\right) \quad (18)$$

$$C2=\frac{-b+\sqrt{b^2-4.a.c}}{2.a} \quad (19)$$

$$C3=\frac{T2.A3.C1}{R2.[k0.T2.A3.C1-C2.(A3.R2(T2.C1)^2]} \quad (20)$$

$$C4= A0-C1-C2-C3 \quad (21)$$

$$R1=\frac{T2}{C2} \quad (22)$$

$$R2=\frac{a2}{(C1.c3.T2)} \quad (23)$$

$$R3=\frac{A3}{T2.R2.C1.C3.C4} \quad (24)$$

The open loop transfer function of the PLL is written as:

$$A(s)=\frac{K_{VCO}.K_{\phi}.H(s)}{s.N_{div}} \quad (25)$$

The equations of the coefficients (a, b, c, a1, a2, k0, c3), and the poles (T1, T2, T3) are found in [6].For an output frequency (Fout)= 2403 MHz, K_{vco}= 210 MHz/v, K_{ϕ}= 50 µA, the ratio of third pole to the first pole (T31)= 0.3, the ratio of fourth pole to the third pole (T43)= 0.4. The values of loop filter components are, C1= 9.85 PF, C2= 182.89 PF, C3=1.6 PF, C4= 1.42 PF, R1= 11.986 KΩ, R2= 28.743 KΩ, R3= 42.17 KΩ.

IV. RESULTS AND DISCUSSION

The analysis and design process were done using Advance Design System Program (ADS). This program gives a simulation results very similar to the implementation results. Fig9depicts the simulated magnitude and phase response of the open loop transfer function. The bandwidth is 200 KHz as expected, and the phase margin isapproximately 50° which seems to be an optimal value.A spectrum analyzer with a Gaussian window, and a 100 KHz resolution bandwidth was used to display the spectrum of the VCO output signal. Fig 10 shows the simulated output spectrum at 2.4 GHz. It can be seen that the synthesized signal is 2403 MHz, and the spectrum is free from any fractional and reference spurs. This means that the used second order modulator is effective in removing the fractional spurs.

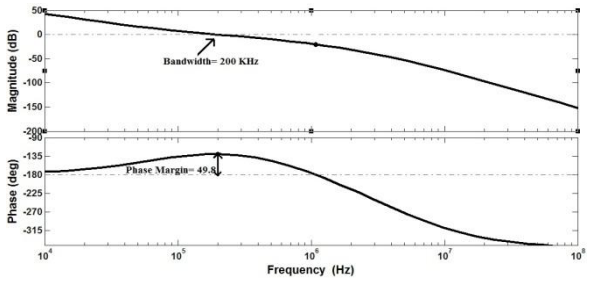

Figure 9. Open Loop Transfer Function

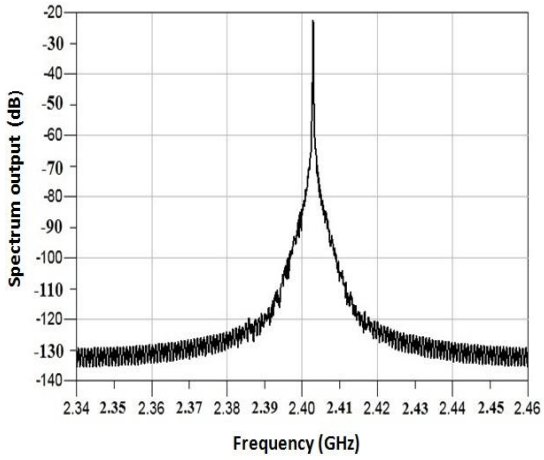

Figure 10. Spectrum output of the Fractional-N Frequency Synthesizer

The phase noise can be calculated from the spectrum output using the following equation [12]:

$$\text{Phase noise}=P_{dBc}-10\log(1.2*RBW)$$

+1.05 dB+1.45 dB (26)

Where P_{dBc} represents the ratio of noise level to carrier level(in dBc), RBW is the resolution bandwidth of the spectrum analyzer, and (1.05, 1.45) are referred to the peak detector average/rms response and logarithmic compression of the noise signal peaks of analyzer respectively. Table 1summarizes the measured phase noise at different offset frequencies.

Table I. Phase noise of a Single Loop Sigma-Delta Fractional N-PLL

Offset frequency (MHz)	0.5	1	3	10	20
Phase noise (dBc/Hz)	-90.4	-96.3	-113	-138.6	-153

The switching time is one of the most important factors in designing fractional-N PLL, since it determines the required time for the synthesized signal to reach a stable state. The switching time depends on the loop filter bandwidth, and when the loop bandwidth is increased the switching time will improve. Fig 11 shows the input voltage of the voltage controlled oscillator versus time. It is clear based on the steady state signal that the switching time is about 6.5 µsec which seems to be a verygood value.

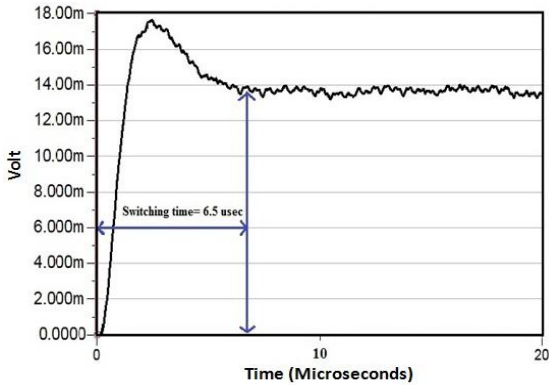

Figure11. Input voltage of the VCO

Table 2 shows a comparison of the present studyversus other works. It is clear that the spurs noise of our design is very small or negligible and can be said that the spectrum is almost free from spurs noise. The phase noise is equal to -90.4 dBc/Hz at 500 KHz offset frequency, which is an acceptable value compared to other designs. The switching time of 6.5 µsec at 2.4 GHz, is a very good value for bluetooth applications. Reference [15] achieves a 2 µsec switching time which is very short time. This is because of high loop filter bandwidth, but high loop bandwidth causes a high spurs noise in the spectrum output as shown by the relatively lower spurs noise suppression value of -34 dBc. Compared to other works, in our fractional-N PLL frequency synthesizer weselected the values of bandwidth and phase margin for loop filter very carefully such that the design offers an excellent switching time, and without spurs noise in the spectrum output.

Table 2. Summary of current research results versus previous published works on fractional-N PLL frequency synthesizer

Parameter/ References	[13]	[14]	[15]	[4]	This work
Output frequency	2.4 GHz	2.4 GHz	2.3 GHz	900 MHz	2.4 GHz
Input frequency (MHz)	12	18	40	8	25
Bandwidth (KHz)	975	100	1000	40	200
Phase noise (dBc/Hz)	-121 @ 3 MHz	-92.5 @ 500 KHz	-122 @ 3 MHz	-122 @ 1 MHz, -135 @ 3 MHz	-90.4 @ 500 KHz, -113 @ 3 MHz
Spurs noise (dBc)	-70	-51	-34	-96	free
Switching time (µsec)	N/A	55	2	N/A	6.5

V.CONCLUSION

This paper illustratesthe design of the fractional-N frequency synthesizer using Sigma-Delta modulation technique. This technique offers a short switching time and a good noise reduction performance. A fourth order passive loop filter offers the best suppression to the quantization noise at high frequencies. The design process of the fourth order passive loop filter is very complicated due to the many factors that must be chosen carefully to have the best performance. The high order single loop Sigma-Delta modulator is conditionally unstable and very complicated in the design, therefore the second order is preferred due to the better stability. The simulation results show that the chosen bandwidth and phase margin yield fast switching time, and the modulator has very good suppression to the fractional spurs.It can be changing the bandwidth or the phase margin of the loop filter To improve the proposed design.

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